

Abstract

A sigma delta circuit is provided having a sigma delta modulator configured to operate according to a first clock signal and a quantizer connected to the sigma delta modulator, where the quantizer is configured to operate according to a second clock signal. In operation, if a small amplitude signal is received by the sigma delta circuit, the circuit is configured to operate at a fixed output frequency. When a large amplitude signal is received, the circuit is configured to adjust to a different frequency to accommodate the larger signal. The second clock signal may be a variable clock signal, where the quantizer operates according to a variable clock signal in order to adjust to different input signals.
